Application No. 09/630,258
Filed: August 1, 2000
Group Art Unit: 2124

REMARKS

Reconsideration of the application, as amended, is respectfully requested. All objections and rejections are respectfully traversed.

The Examiner has objected to the abbreviation FFT in claims 1, 5 and 8. In response, the claims have been amended to refer to "fast Fourier transform". In view of this amendment, it is believed that the objection has been overcome.

The Examiner has objected to the inclusion of an "x" in claim 2. In response the "x" has been removed from claim 2. In view of this amendment, it is believed that the objection has been overcome.

Claims 1-8 are currently pending in the application. Claims 1, 5 and 8 are independent.

The Examiner has rejected claim 2 under 35 USC § 112, second paragraph as being indefinite. With respect to the rejection under 35 USC § 112, second paragraph, the Applicant has amended claim 2 to specify that the time-ordered input data stored in the first memory is replaced by the calculation-ordered butterfly output data stored in the third memory. In view of such amendment, it is believe the rejection under 35 USC § 112 has been overcome.

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Claims 1-8 stand rejected under 35 USC § 102(e) as being anticipated by Nakai et al., ("Nakai"). With respect to the rejection under 35 USC § 102(e), the Applicant has amended claims 1, 5, and 8 to specify that the time-ordered input data received is sequentially stored in the first memory in the time-order in which the input data is received. In addition, for each stage of the fast Fourier transform (FFT), the butterfly output data is stored sequentially in the order that the butterfly data is calculated. Thus at each butterfly stage within the FFT, the data is stored in sequential memory locations, i.e., in a unity-stride manner. As discussed in the specification, the storage of data in a unity-stride manner is one advantage of the claimed invention and helps to increase the speed of the FFT system while reducing the complexity of the FFT system.

In contrast to the claimed invention, Nakai fails to teach or fairly suggest the storage of data in a unity stride fashion as claimed in the present invention. In particular, Figs. 6, 7, and 33 of Nakai depict an FFT signal flow graph and the corresponding memory locations that are used to store the input data and output data for each butterfly calculator within each FFT processing stage. Nakai teaches that the input data is stored in a bit-reversed manner that is a function of the radix of the butterfly stage and the number of data being processed and not in the time

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order in which the input data was received. Thus, Nakai teaches away from the presently disclosed and claimed invention.

More specifically, in Figs. 6 and 7 of Nakai, the input data is stored sequentially ordered as x0, x2, x4, x6, x1, x3, x5, and x7, where 0, 1, 2, ... 7 represent the time order of the input data. In Fig. 33 the input data is stored sequentially ordered as x0, x4, x2, x6, x1, x5, x3, and x7, where 0, 1, 2, 3, 4, 5, 6, 7 represent the time order of the input data. In contrast in the claimed invention, the input data is sequentially stored in the received time order as x0, x1, x2, x3, x4, x5, x6, and x7.

In addition, in some stages of the FFT processor taught in Nakai, the output data of a butterfly calculator stage within the FFT processor is not stored in the order that the output data is calculated. For example, in Fig. 6 the output data of the first and butterfly operations in the FFT Processing [i] and [i+2] are not stored in the order in which the output data is calculated. In particular, in Fig. 6 the output data of the second butterfly calculator in the FFT Processing [i] is stored as X0, X1, X2, X3, X4, X5, X6, and X7 and is then rearranged within the memory. However, the order the data is calculated in, and stored sequentially in as in the claimed invention is: X0, X4, X1, X5, X2, X6, X3, and X7.

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Similarly, in Fig. 7, the output data of the FFT processing [i] and [i+4] are not stored in the order in which the output data is calculated. As depicted in Fig. 7, there are three butterfly operations, each using two stages of butterfly operation stages, one each in the FFT Processing [i], FFT Processing [i+2], and FFT Processing [i+4]. In the first butterfly operation in FFT Processing [i] the architecture is the same as depicted in Fig. 6 and the explanation for Fig. 6 is applied to this stage as well. The second butterfly operation in FFT Processing [i+2] includes two butterfly stages and wherein the first butterfly stage stores the output data sequentially but not in the order in which the data was calculated. As shown in Fig. 7, the data is sequentially stored as depicted and is represented as X0-X7. However in the claimed invention, the output data would be stored in the order the data is calculated in, i.e., X0, X2, X4, X6, X1, X3, X5, and X7. In the third FFT processing stage, FFT Processing [i+4], both of the butterfly calculators store the data sequentially but do not store the data in the calculated order. The first butterfly stage stores the data as X0-X7, when the calculation order of the output data is X0, X1, X4, X5, X2, X3, X6, and X7. The second butterfly calculator of the third butterfly operation stores the output data as X0, X2, X4, X6, X1, X3, X5, and X7, when the actual

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calculation order of the output data would be X0, X4, X2, X6, X1, X5, X3, and X7.

Similarly as to the FFT signal flow diagrams depicted in Figs. 6 and 7, the FFT signal flow graph depicted in Fig. 33 fails to teach or suggest that each stage with in the butterfly operation stores the data in the order in which it was calculated. In particular as depicted in Fig. 33 the output data of second and third butterfly calculators of the first butterfly operation, FFT Processing [i] and the first and second butterfly calculators of the second butterfly operation, FFT Processing [i+2] fail to sequentially store the output data in the order in which it is calculated.

Accordingly, the Applicants assert that Nakai fails to teach or suggest that an FFT store the time-ordered input data sequentially in the time-order in which the input data is received. Furthermore, the Applicants assert that Nakai fails to teach or suggest that each stage within an FFT butterfly operation stores the output data sequentially in the order in which the data is calculated. Therefore, the Applicant asserts that claim 1 is patentably distinct over the Nakai reference and respectfully requests the reconsideration and allowance of claim 1. Claims 2-4 depend from claim 1 and are patentable for at least the same reasons as claim 1.

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For the reasons set forth above with respect to claim 1, the Applicants assert that independent claims 5 and 8 are also patentably distinct over the Nakai reference and respectfully requests the reconsideration and allowance of claim 5. Claims 6 and 7 depend from claim 5 and are patentable for at least the same reasons as claim 5.

In view of the foregoing remarks and amendments, the Applicants respectfully submit that all present claims and the Application are in condition for allowance and such action is respectfully solicited.

The Examiner is encouraged to telephone the undersigned attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

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ABSTRACT OF THE DISCLOSURE

A method for computing an out of place FFT in which each stage of the FFT has an identical signal flow geometry. In each stage of the presently disclosed FFT method the group loop has been eliminated, the twiddle factor data is stored in bit-reversed manner, and the output data values are stored with a unity stride.